

Remarks

Applicant thanks Examiner Mandala again for his careful examination and clear explanation of the claim rejections. In response, applicant amends claim 8 to describe the invention more clearly. Regarding claims 7, and 9-11, applicant respectfully traverses the reason for rejection cited in the Office action and wishes to point out the particular enablement descriptions in the specification:

1. Claim 7 describes an integrated circuit structure that comprises the following limitations:
 - a. a gate structure formed on a body of semiconductor material;
 - b. an insulating layer formed opposite the gate structure beneath the semiconductor material;
 - c. a conducting region of sublithographic width within the insulating layer beneath the gate structure.

One embodiment of the invention in claim 1 is described on page 9, paragraph 1 of the specification. This paragraph is copied here:

Figure 3 shows a substrate 302 covered by a layer of insulating material 304, preferably oxide. A trench 306 is etched in the oxide, followed by formation of sidewalls 308 in the trench. A conducting material 310 (preferably polysilicon) is deposited in the trench. (Note that in some embodiments, an electrical interconnect is also present, connecting the trench fill material to another voltage element.) The surface is then planarized and covered by another insulating layer of oxide 312, followed by formation of the active area 314 and the gate 316.

It is clear from this paragraph that element 316 of this embodiment corresponds to the gate element in (a) of claim 1; element 314 corresponds to the “a body of semiconductor material” element in (a) of claim 1; element 304 corresponds to “an insulating layer” element in (b) of claim 1; element 310 corresponds to the “a conducting region” element in (c) of claim 1; and element 304 corresponds to “the insulating layer” element in (c) of claim 1.

The argument for rejecting claims 7 – 12 is that “[t]he specification and drawings teach of a conductor on a semiconductor body where the insulating layer is above the conductor and there is

an additional insulating layer beneath the conductor, but nowhere is it taught to be below the semiconductor body.” However, in an embodiment depicted in Figure 3, element 314 represents a semiconductor body and element 312 represents an insulating layer below the semiconductor body. Therefore, the disclosure is enabling and every element of limitation in claim 7 is disclosed in the specification and the drawing figures. Applicant respectfully requests that the 112 rejection against claim 7 be withdrawn.

2. Applicant amends claim 8 so it describes the invention more clearly. In the embodiment depicted in figure 3, the semiconductor material element that makes contact with the conductive region element 310 is the element 302. Because the disclosure is enabling and the additional element of limitation in claim 8 is disclosed in the specification and the drawing figure. Applicant respectfully requests that the 112 rejection against claim 8 be withdrawn.

3. Claim 9 further limits the structure of the conductive region to be in a trench with sidewalls. This is also clearly disclosed in the specification, for example, in the second and third paragraphs on page 5 of the specification and in drawing figures 1b, 1c, and 1d. Because the disclosure is enabling and the additional element of limitations in claim 9 are disclosed in the specification and the drawing figures. Applicant respectfully requests that the 112 rejection against claim 9 be withdrawn.

4. Claim 10 further limits the semiconductor material to silicon. This is disclosed in the specification, for example, in paragraph 3 on page 6 bridging page 7.

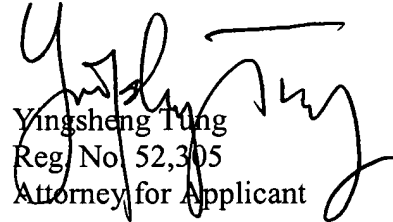
5. Claim 11 further limits the conductive material to be separated from the semiconductor material. This is also disclosed, for example, in drawing figure 3, where element 312 is an insulating layer separating the conductive region 310 from the semiconductor 314.

6. The objection against drawings cites missing structure elements such as the gate structure and the insulating layer beneath the semiconductor body. As explained above, one embodiment of such a structure is depicted in drawing figure 3 where a gate structure is the element 310 and an insulating layer is element 312.

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In conclusion, applicant respectfully submits that the disclosure is enabling and all elements in the claims are disclosed in the specification. Applicant respectfully requests withdrawing of the rejections and further examination of this application.

Respectfully submitted,



Yingsheng Tung
Reg. No. 52,305
Attorney for Applicant

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, Texas 75265
(972) 917-5355